into a plurality of shift registers, and each divided shift register being time-divisionally driven in synchronization with the input data, as recited in claim 1.

Moreover, none of the applied references disclose or suggest at least an n-stage shift register being divided into first and second shift registers each having n/2 stages, one of the first and second shift registers performing a shift operation at a rising edge of a shift clock, and the other of the first and second shift registers performing a shift operation at a falling edge of the shift clock, as recited in claim 2, and similarly recited in claim 3.

Specifically, the Office Action asserts that Tomimitsu discloses that an output of each output stage of the shift register is multiplied (via multipliers 321-32m and 341-34m; see column 4, lines 21-26) by a filter coefficient and added (by adders 35 and 36), the end-stage shift register being divided into a plurality of shift registers (filters 51 and 52). However, Figures 4 and 5 of Tomimitsu disclose the structure of parallel filters, e.g., an even-order filter and an odd-order filter. See col. 4, lines 17-41. The parallel filters are not a shift register (and do not perform the same function) as recited in claims 1-3.

Although a shift register 90 is shown in Figures 9 and 10 of Tomimitsu, the shift register is not divided into a plurality of shift registers and does not provide an output that is multiplied by a filter coefficient and then added by an adder. Moreover, the shift register 90 in Tomimitsu is not divided into first and second shift registers each having n/2 stages, with one of the registers performing a shift operation at a rising edge of a shift clock, and the other register performing a shift operation at a falling edge of the shift clock. On the contrary, nowhere in Tomimitsu are these features disclosed or suggested. Thus, Tomimitsu fails to disclose each and every feature of the claimed invention.

Matsudera discloses a semiconductor memory device.

Lomp discloses a CDMA modem with a transmitter.

Tayebi discloses a system and method for communicating radio frequency signals.

Because Matsudera, Lomp and Tayebi fail to compensate for deficiencies in Tomimitsu, it would not have been obvious to combine the applied references to arrive at the claimed invention. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-6 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Richard S. Elias
Registration No. 48,806

JAO:RSE/eks

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OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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